

LSI LOGIC

**FAX COVER SHEET**

**LSI LOGIC CORPORATION**  
**Office of General Counsel**  
**1621 Barber Lane**  
**M/S D-106**  
**Milpitas, CA 95035**  
**Fax: (408) 433-7460**

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**Date:** May 24, 2004  
**To** **Name:** USPTO – Box: Status Request  
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**From:** **Name:** Manu Kashyap, Intellectual Property Paralegal  
**Corporate Legal Dept.**  
**Telephone:** (408) 433-7475  
**Fax:** (408) 433-7460  
**Re:** 10/021,696

Number of Pages Including this Page 3

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**MESSAGE:**

**US Serial No.: 10/021,696**  
**Filing Date: October 30, 2001**  
**Group Art Unit: 2825**  
**Docket No: 01-490**  
**Examiner: Vuthe Siek**  
**Request for Status**

Please notify us immediately if any pages are not received.

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Michael Eneboe et. al.

Serial No. :

10/021,696

Filed :

October 30, 2001

For :System and Method for Optimizing  
an Integrated Circuit DesignGroup Art Unit :

2825

Examiner :

Siek, Vuthe

Atty Docket :

/ 01-490

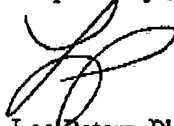
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OFFICIALSTATUS REQUESTCommissioner for Patents  
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Sir:

Applicants request a status of the above referenced application. Please mail the status notification to the address stated below.

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1621 Barber Lane, MS D-106  
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[+1] 408-433-7475Date: 5-24-04

Respectfully submitted,



Leo Peters, Ph: [+1] 408-433-7475

Reg. No. 33,562